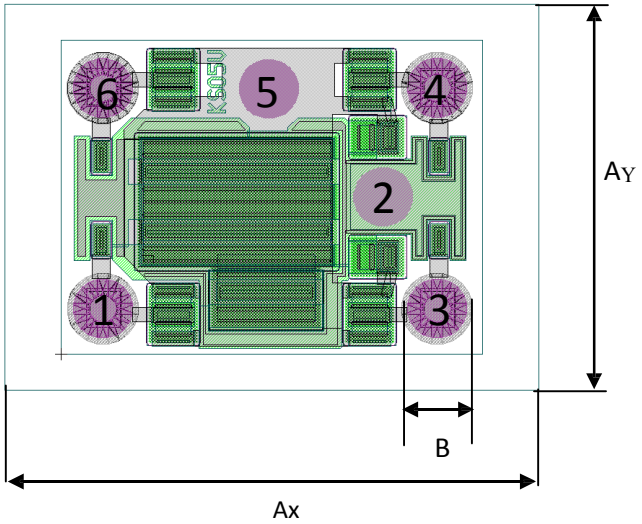

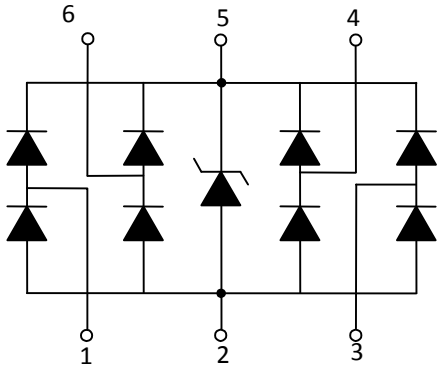

Mechanical data: A_x= 800um, A_Y=580um,B=90um

Schematic and pinning diagram.

Chip thickness: a)KS-05V4M4A: 203+/-12um.
b) KS-05V4M4B: without grinding 460+/-20um
c) KS-05V4M4C: agreement with the customer

Pin#	Description
1, 3, 4,6	I/O-Lines
5	Vcc
2	GND

Scribe Line width -60um.
Top Metal: Al – thickness4,0+/-0,4um;
Back side – Ti-Ni-Ag– thickness 0,1-0,3-0,5um or without metallization

Probing: a) sampling testing : no bad dice inking, guaranteed good dice quantity ≥93%
b) 100% testing (if agreed with customer): wafer mapping data, no bad dice inking

Limiting values

Parameter	Symbol	Conditions	Value	Unit
DC input voltage range	$V_{I/O}$	-	+5.5max	V
Peak Pulse Power	Ppp	t_p =8/20uS	48	W
Peak Pulse Current	Ipp	t_p =8/20uS	4,0	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level4.	±8.0(Contact)	kV
Max. junction temperature	T_j	-	+125	°C

Characteristics(Tj=25ºC)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{lkg}	Diode reverses leakage current. Pins 1, 3, 4, 6 to Pin 2.	V=+5,0V	-	-	0,2	uA
V_{BR}	Zener diode breakdown voltage. Pin 5 to Pin 2.	I_Z=1mA	6,1	6,7	8,0	V
V_{SB}	Snap Back Voltage Pin 5 to Pin 2.	I_{SB}=50mA	-	5,8	-	V
V_F	Forward voltage. Pin 2 to Pin 5.	I_F=1mA	-	0,7	-	V
Vcl*	Clamping Voltage	Ipp=1A,t=8/20uS; Ipp=4A,t=8/20uS	- -	- -	8,0 12,0	V
$C_{I/O}$	Pin capacitance. Pins 1, 3, 4, 6 to Pin2.	Vdc=0 V; f=1MHz.	-	0,65	0,8	pF
$C_{I/O-I/O}$	Any I/O pin to I/O.	Vdc=0 V; f=1MHz.	-	0,3	-	pF

*- For Device testing

Fig1: TVS characteristic curve