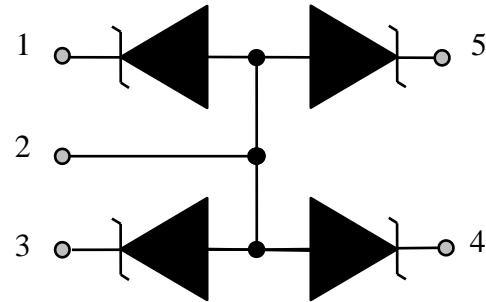
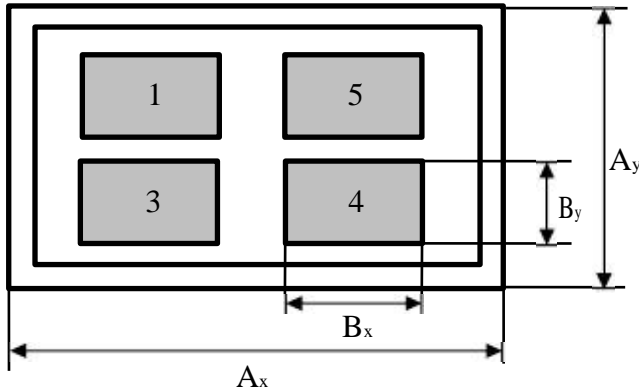


KS-3,3V4L1

Chip low capacitance 4- fold ESD protection diode.



Mechanical date: $A_x=1400$ um, $A_y=800$ um.
 $B_x=290$ um, $B_y=200$ um

Chip thickness: 230+/-20um

Scribe Line width - 60um.

Top Metal: Al - for wire bonding.

Back side - Anode: Ti-Ni-Ag for soldering.

Schematic and pinning diagram.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	3,3	V
Peak Pulse Power	P_{pp}	$t_p=8/20\mu s$	200*	W
Peak Pulse Current	I_{pp}	$t_p=8/20\mu s$	12,0*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>15 (Contact); >25 (Air).	kV
Max.junction temperature	T_j	-	+125	°C

Characteristics ($T_j=25^\circ C$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SB}	Snap-Back Voltage	$I_R=50mA$	2,85	-	-	V
I_R	Reverse leakage current	$V=3,3V$	-	-	0,4	uA
V_{PT}	Punch-Through voltage	$I_R=1,5\mu A$	3.55	-	-	V
V_F	Forward voltage (pins 1, 3, 4, 6 to pins 2,5)	$I_F=1A$; $t_p=8/20\mu s$	-	-	1,7*	V
V_{CL}	Clamping voltage (pins 1, 3, 4, 6 to pins 2,5)	$I_{pp}=1A$; $t_p=8/20\mu s$	-	-	4,5*	M
		$I_{pp}=5A$; $t_p=8/20\mu s$	-	-	6,8*	
		$I_{pp}=12A$; $t_p=8/20\mu s$	-	-	8,7*	
C_j	Junction Capacitance to ground (pins 1, 3, 4, 6 to pins 2,5)	$V_R=0$ V, $f=1MHz$	-	-	40	pF

*- For Device testing