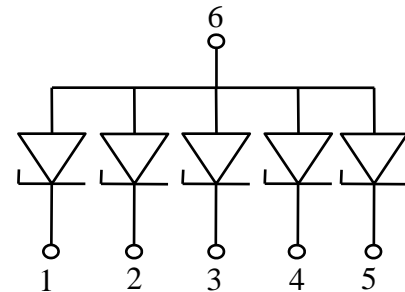
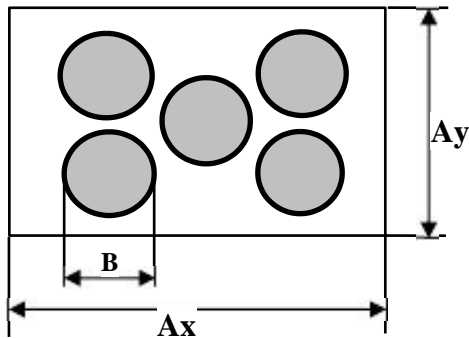


KS-5.0V5L1, KS-5.0V5L2

Chip low capacitance 5- fold ESD protection diode.



Mechanical date: $A_x=480\mu\text{m}$, $A_y=370\mu\text{m}$, $B=90\mu\text{m}$

Chip thickness: a) $230\pm 20\mu\text{m}$ – for KS-5,0V5L1;
b) $138\pm 12\mu\text{m}$ – for KS-5,0V5L2.

Scribe Line width - $60\mu\text{m}$.

Top Metal: Al - for wire bonding, $d=2.2\pm 0.2\mu\text{m}$.

Back side - Anode: Ti-Ni-Ag for soldering.

Schematic and pinning diagram.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5	V
Peak Pulse Power	P_{pp}	$t_p=8/20\mu\text{s}$	25*	W
Peak Pulse Current	I_{pp}	$t_p=8/20\mu\text{s}$	2.5*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>8 (Contact); >15 (Air).	kV
Max.junction temperature	T_j	-	+150	°C

Characteristics ($T_j=25^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Breakdown voltage	$I_R=1\text{mA}$	6.45	-	7.15	V
I_R	Reverse leakage current	$V=5\text{V}$	-	5	25	nA
V_{CL}	Clamping Voltage	$I_{pp}=1.0\text{A}$, $t_p=8/20\mu\text{s}$ $I_{pp}=2.5\text{A}$, $t_p=8/20\mu\text{s}$	-	-	10* 12*	V
C_j	Diode capacitance	$V_R=0\text{V}$, $f=1\text{MHz}$	-	16	19	pF

*- For Device testing