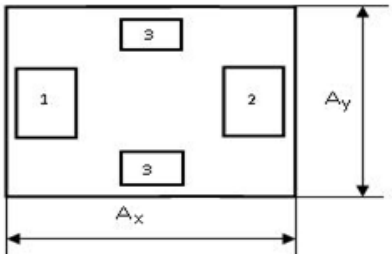
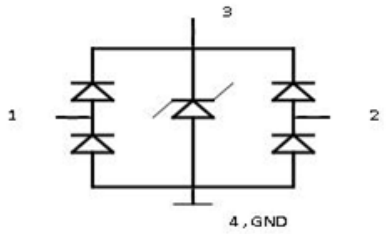


Pin 4 – back side – GND



Mechanical data: A_x= 490um, A_y=300um

Schematic and pinning diagram

Pad Size for Pin 1, 2 - 90 *80 um.

Pad Size for Pin 3 -120*80 um.

Chip thickness: a) 138+/-12um on 4" wafer – for KSR-5.0V2M6A .

b) 470+/-20 um on 4" wafer – for KSR-5.0V2M6B.

c) 655+/-20um on 6" wafer – for KSR-5.0V2M6C.

Scribe Line width - 60um.

Top Metal: Al - for wire bonding.

Back side - Anode: a) Ti-Ni-Ag for soldering – for KSR-5.0V2M6A .

b) without metallization – for KSR-5.0V2M6B.

c) without metallization – for KSR-5.0V2M6C.

Probing: a) sampling testing: no bad dice inking guaranteed good dice quantity≥93%;

b) 100% testing (if agreed with customer): wafer mapping data no bad dice inking.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5	V
Peak Pulse Power	P_{pp}	tp=8/20us	100*	W
Peak Pulse Current	I_{pp}	tp=8/20us	5*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>8 (Contact); >15 (Air).	kV
Max.junction temperature	Tj	-	+150	ºC

Characteristics **(Ta=25ºC)**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Breakdown voltage, I/O to GND.	I_R=1mA	6,1	7,0	-	V
I_R	Reverse leakage current	V=5V	-		0,9	uA
V_F	Forward voltage	I_F=15mA	-	-	1,15	V
V_{CL}	Clamping Voltage, I/O to GND	I_{pp}=1.0A, t_p=8/20us I_{pp}=5.0A, t_p=8/20us	-	-	10* 20*	V
C_J	Capacitance. I/O to Ground	V_R=0 V, f =1MHz	-	0,55	0,8	pF
C_J	Capacitance between I/O pins.	V_R=0 V, f =1MHz	-	0,25	0,4	pF

*- For Device testing