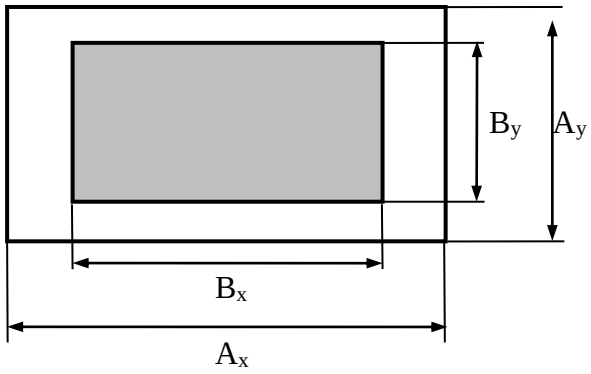
VSP-MIKRON

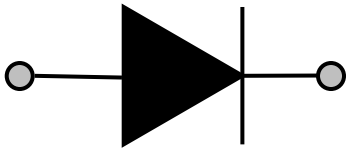
Rev.1. Sept 2010.

LCD-150P3

PRELIMINARY.

Dual chip low capacitance diode on P+ type substrate.





Mechanical date: A_x=580umA_y=380um.
B_x=410B_y=210um
Chip thickness: 180+/-20um
Scribe Line width - 60um.
Top Side – Cathode. Al metallisation for wire bonding
Thickness Al – 2.2+/-0.2 um
Back side - Anode: Ti-Ni-Ag for soldering.

Schematic and pinning diagram.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Max. Peak Pulse Current	I_{FM}	t_p=8/20us	24,0*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>15 (Contact); >25 (Air).	kV
Max.junction temperature	T_j	-	+150	ºC

Characteristics (Tj=25ºC)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Breakdown voltage	I_R=1mA	50,0	-	-	V
I_R	Reverse leakage current	V_R=50,0V	-	-	0,9	uA
V_F	Peak forward voltage	I_F=1,0A, t_p= 8/20uS I_F=5,0A, t_p=8/20uS I_F=24,0A, t_p=8/20uS	- - -	- - -	1,0* 2.5* 6.0*	V
C_J	Diode capacitance	V_R=0 V, f =1MHz	-	5.0	-	pF

*- For Device testing