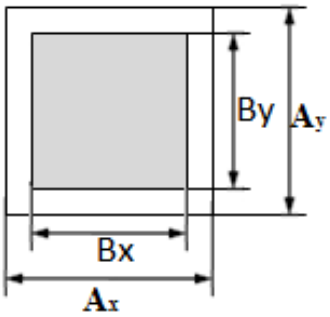

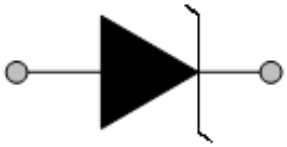

Mechanical date: $A_x = A_y$=710um
Bx=By=550um

Schematic and pinning diagram

Chip thickness: 635+/-20um without griding
Scribe Line width - 40um.
Top Metal: AL with Ti under layer metallization for wire bond, thickness 2,2-2,4um.
Back side - Anode: without metallization
Top Side (Cathode) - pin 1, **Back Side (Anode)** - pin 2.
Sampling testing: no bad dice inking;
guaranteed good dice quantity≥93%.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	7,0	V
Peak Pulse Power	P_{pp}	t_p=8/20us	1400*	W
Peak Pulse Current	I_{pp}	t_p=8/20us	80*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	>±30kV(Contact); >±30kV (Air).	kV
Max.junction temperature	T_j	-	+150	ºC

Characteristics **(Tj=25ºC)**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BR}	Breakdown voltage	I_R=1mA	7,5	-	10	V
I_R	Reverse leakage current	V=7.0V	-	-	1	uA
V_F	Forward voltage	I_F=10mA	0,6	-	1,2	V
V_{CL}	Clamping Voltage	I_{pp}=1.0A, t_p=8/20us I_{pp}=20A, t_p=8/20us I_{pp}=80A, t_p=8/20us	-	-	9,7* 11,5* 17,5*	V
C_J	Diode capacitance	V_R=0 V, f =1MHz	-		600	pF

*- For Device testing