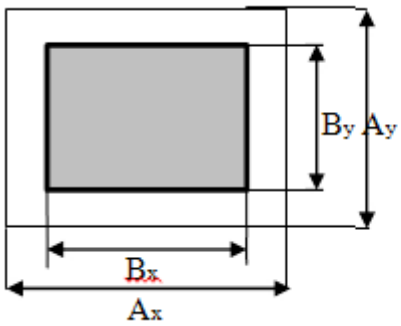

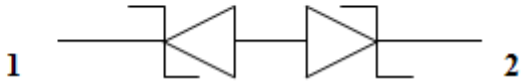

Mechanical date: $A_x=A_y=210$um
$B_x=B_y=85$um

Schematic and pinning diagram

Chip thickness: 635 +/-20um
Scribe Line width - 40um.
Top Metal: Al – for wire bonding, d=2.2+/-0.2um
Back side : without metallization
Top Side - pin 1, **Back Side** - pin 2.
Probing: sampling testing: no bad dice inking, guaranteed good dice quantity≥95%.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	5	V
Peak Pulse Power	P_{pp}	t_p=8/20us	35*	W
Peak Pulse Current	I_{pp}	t_p=8/20us	2*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	+/-8 (Contact); +/-15 (Air).	kV
Max.junction temperature	T_j	-	+150	ºC

Characteristics **(Ta=25ºC)**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_R	Diode reverse leakage current.	V=±5,0 V	-	-	90	nA
V_{BR}	Breakdown voltage. Pin 1 to 2 or Pin2 to 1.	I_R=1mA	5,6	-	9,4	V
C_j	Diode capacitance .	F=1MHz, V_{dc}=0 V.	-	3,0	3,5	pF
V_{CL}	lamping voltage	I_{pp}=1,0A; I_{pp}= 2,0A; t_p= 8/20uS .	- -	- -	10,0* 13,0*	V

*- For Device testing