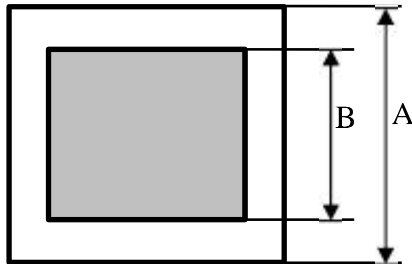
VSP-MIKRON

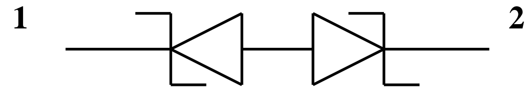
RoHS

Rev.4. June 2014

SMB-3,3L41, SMB-3,3L42

Chip Bi - directional TVS diode in wafer form, 4 inch.





Mechanical data: A_x=A_y=280um, B_x= B_y= 100um

Schematic and pinning diagram.

Chip thickness: a) 138+/-12um – for SMB-3,3L41;
b) 470+/-20um – for SMB-3,3L42.

Scribe Line width - 60um.

Top Metal: Al - for wire bonding, d=2.2+/-0.2 um.

Back side: a) Ti-Ni-Ag for Soldering – for SMB-3,3L41;
b) not grinded, without metallization – for SMB-3,3L42.

Top Side - pin 1, **Back Side** - pin 2.

Sampling testing: no bad dice inking;
guaranteed good dice quantity≥95%.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-off voltage	V_{RWM}	-	3,3	V
Peak Pulse Power	P_{pp}	t_p=8/20us	90*	W
Peak Pulse Current	I_{pp}	t_p=8/20us	5,0*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4.	+/-8 (Contact); +/-15 (Air).	kV
Max.junction temperature	T_j	-	+150	°C

Characteristics (Tj=25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_R	Diode reverse leakage current.	V=±3,3 V	-	0,05	0,40	uA
V_{PT}	Punch-Through Voltage	I_{PT}=2uA	3,5	-	-	V
Vsb	Snap-Back Voltage	Isb=50mA	2,8	-	5,5	V
C_j	Diode capacitance .	f=1MHz, V_{dc}=0 V. f=1MHz, Vdc=3,3V	- -	- 10,0	15,0 -	pF
V_{CL}	Clamping voltage	I_{pp}=1,0A; t_p= 8/20uS . I_{pp}= 5,0A;t_p= 8/20uS .	- -	- -	8,0* 18,0*	V

* For Device testing.